AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A semiconductor integrated circuit comprising:

a rewritable nonvolatile memory for storing first trimming data formed on the semiconductor integrated circuit; ~~and~~

an interface circuit for test coupled to said nonvolatile memory,

a digital to analog converter coupled to the nonvolatile memory; and

a register coupled to the digital to analog converter for storing second trimming data;

wherein the digital to analog converter receives the stored first trimming data from said nonvolatile memory and receives the second trimming data from the register and outputs adjustment data, and

wherein said nonvolatile memory stores said trimming~~adjustment~~ data for correcting a change in circuit characteristics which occurs due to variations in electronic

parts or devices, ~~can be written into said nonvolatile memory~~ via said interface circuit for test.

2. (Currently amended) The semiconductor integrated circuit according to claim 1, further comprising:

a terminal for outputting the adjustment data ~~stored in said nonvolatile memory or a value obtained by D/A converting the adjustment data~~.

3. (Currently amended) The semiconductor integrated circuit according to claim 1, further comprising:

a microprocessor ~~for control~~ for executing [[a]] control in accordance with [[a]] commands of a program; and

a program memory for storing said program commands executed by the microprocessor,

wherein said microprocessor reads the adjustment data stored in said nonvolatile ~~memory can be read by said microcomputer~~.

4. (Original) The semiconductor integrated circuit according to claim 1, wherein said electronic part is a quartz oscillator, and said adjustment data is data for adjusting an oscillation frequency of an oscillating circuit including said quartz oscillator.

5. (Currently amended) An electronic system comprising:

an electronic part;

a first semiconductor integrated circuit including:

a first nonvolatile memory formed on the said first semiconductor integrated circuit,

a microprocessor coupled to the first nonvolatile memory and ~~for control for executing a control in accordance with a command of a program~~configured to execute a sequence of programmed instructions,

an interface circuit for test coupled to the first nonvolatile memory, ~~and~~

~~———————~~a second nonvolatile memory coupled to the microprocessor for storing said ~~program~~ instructions executed by the microprocessor,

wherein said first nonvolatile memory stores~~ing~~ ~~adjustment~~first trimming data for correcting a change in circuit characteristics which occurs due to variations in said electronic part[[s]]; ~~and~~

a digital to analog converter coupled to the first nonvolatile memory; and

a register coupled to the digital to analog converter for storing second trimming data;

wherein the digital to analog converter receives the stored first trimming data from said first nonvolatile memory and receives the second trimming data from the lower bit register and outputs adjustment data; and

a substrate over which the electronic part and the first semiconductor integrated circuit ~~being~~ are mounted,

wherein said ~~adjustment data stored in said~~ first nonvolatile memory is rewritable for storing updated first trimming data.

6. (Currently amended) The electronic system according to claim 5, wherein ~~said adjustment data can be written in~~ said first nonvolatile memory stores said first trimming data received via a terminal, wherein the terminal ~~also serving as~~ is a test terminal provided over said substrate.

7. (Currently amended) The electronic system according to claim 5, wherein said first semiconductor integrated circuit has an interface circuit for test, and ~~said adjustment data can be written in~~wherein said first nonvolatile memory stores said adjustment data received via said interface circuit for test.

8. (Original) The electronic system according to claim 5, wherein said second nonvolatile memory is a mask ROM.

9. (Original) The electronic system according to claim 5, wherein said electronic part is a quartz oscillator, and said adjustment data is data for adjusting an oscillation frequency of an oscillating circuit including said quartz oscillator.

10. (Currently amended) The electronic system according to claim 9, further comprising a second semiconductor integrated circuit in which a device is formed that provides ~~for constructing~~ an oscillating circuit when coupled to~~together with~~ said quartz oscillator ~~is formed~~,

wherein a clock signal generated by said second semiconductor integrated circuit is supplied as a reference clock signal to said first semiconductor integrated circuit.

11. (Currently amended) The electronic system according to claim 10, wherein said first semiconductor integrated circuit is a semiconductor integrated circuit ~~for baseband~~ for performing a baseband signal process for communication, and said second semiconductor integrated circuit is a

semiconductor integrated circuit ~~for RF~~ having a radio frequency transmission/reception function.

12. (Currently amended) A semiconductor integrated circuit comprising:

a rewritable nonvolatile memory formed on the semiconductor integrated circuit; ~~and~~

an interface circuit for test coupled to the nonvolatile memory,

a digital to analog converter coupled to the nonvolatile memory; and

a register coupled to the digital to analog converter for storing second trimming data;

wherein the digital to analog converter receives the stored first trimming data from said nonvolatile memory and receives the second trimming data from the register and outputs adjustment data, and

wherein said nonvolatile memory stores said first trimming ~~adjustment~~ data for correcting a change in circuit characteristics caused by variations in electronic parts or devices, and data peculiar to the semiconductor integrated circuit, ~~can be written to said nonvolatile memory~~ via said interface circuit for test.

13. (Original) The semiconductor integrated circuit according to claim 12, wherein said electronic part is a quartz oscillator, and said adjustment data is data for adjusting oscillation frequency of an oscillating circuit including said quartz oscillator.

14. (New) The semiconductor integrated circuit according to claim 1, wherein the first trimming data is upper bit trimming data and the second trimming data is lower bit trimming data.

15. (New) The semiconductor integrated circuit according to claim 14, wherein the register is coupled to the microprocessor and the microprocessor determines the lower bit trimming data to synchronize a slave clock to a master clock.

16. (New) The semiconductor integrated circuit according to claim 5, wherein the first trimming data is upper bit trimming data and the second trimming data is lower bit trimming data.

17. (New) The electronic system according to claim 16, wherein the register is coupled to the microprocessor and

the microprocessor determines the lower bit trimming data to synchronize a slave clock to a master clock.

18. (New) The semiconductor integrated circuit according to claim 12, wherein the second trimming data is lower bit trimming data.

19. (New) The semiconductor integrated circuit according to claim 18, wherein the register is coupled to the microprocessor and the microprocessor determines the lower bit trimming data to synchronize a slave clock to a master clock.